H8x SPI Adapter
(WIZ850io/25LC512)
Theory of Operation
07/15/19

Basic SPI

MOSI - Master Out Slave In - carries serial data from the H8/H89 to the SPI devices. MISO - Master In Slave Out - carries serial data from the SPI devices to the H8/H89. SCLK clocks data over MOSI and MISO, simultaneously. The only way to read data is to clock-out (write) data. SPI devices will ignore written data while they are in a read phase. Likewise, the H8/H89 ignores read data while writing.

The SPI adapter will clock 8 bits when either an IN or OUT instruction (on the data port) is performed, however in the case of IN there is no data loaded into the output (write) shift register. Also, in the case of IN, there is a delay for when the input data is available, since the shifting occurs *after* the IN instruction. Since SPI devices require a command in order to perform an operation, there is at least one OUT (the command) performed prior to any INs. The data from the first IN instruction after writing the command (and parameters) will be ignored, as it contains no meaningful value. As an example, a command to read 16 bytes will consist of 17 IN instructions, with data from the first being discarded.

Devices share the same MOSI, MISO, and SCLK signals, but each device has it's own /SCS (or /SS) signal, to select them as active. The absence of this select signal causes the SPI device to ignore its serial input line and tri-state its serial output line.

The general protocol for communicating with an SPI device is:

1. Set the select bit for the desired device to "1"
2. Output one or more bytes for the command/parameter(s)
3. Either output or input data bytes, depending on command
4. Clear the select bit

Note that step 4 is often required by the devices in order to execute a command (the command may not start until after step 4). Only one command may be issued per select cycle.

Most devices (the two used here) support an “auto increment” feature, such that the size of data transfers need not be specified in the command. The H8/H89 simply clears the /SCS signal after the last desired data byte. There may, however, be internal limitations on the devices such as page sizes or register bank boundaries.

Adapter Hardware Operation

The /SCS (or /SS) signals are controlled by the 74LS175 latch, which is loaded by OUT on the control port. Bit 0 is /SCS for the WIZ850io. Bit 1 is the /SS for the 25LC512 NVRAM chip. System /RESET forces both (all) bits to "0".

Serial data shifting is controlled by the 74LS161 counter, and associated circuitry. A system /RESET will, via the /SCS signals, preload 1111b into the counter. This forces Q3 to "1" which forces preset on the set of 74LS74 flipflops. The Q output of the last flipflop drives the SCLK-DIS (serial clock disable) signal, which prevents the system CPU clock from reaching the shift registers. This condition will persist as long as no SPI device is selected.

Enabling /SCS for one of the devices (it is software's responsibility to ensure only one device is selected) releases the preload (/PE) on the 74LS161, but no clocking will begin since Q3 remains "1".

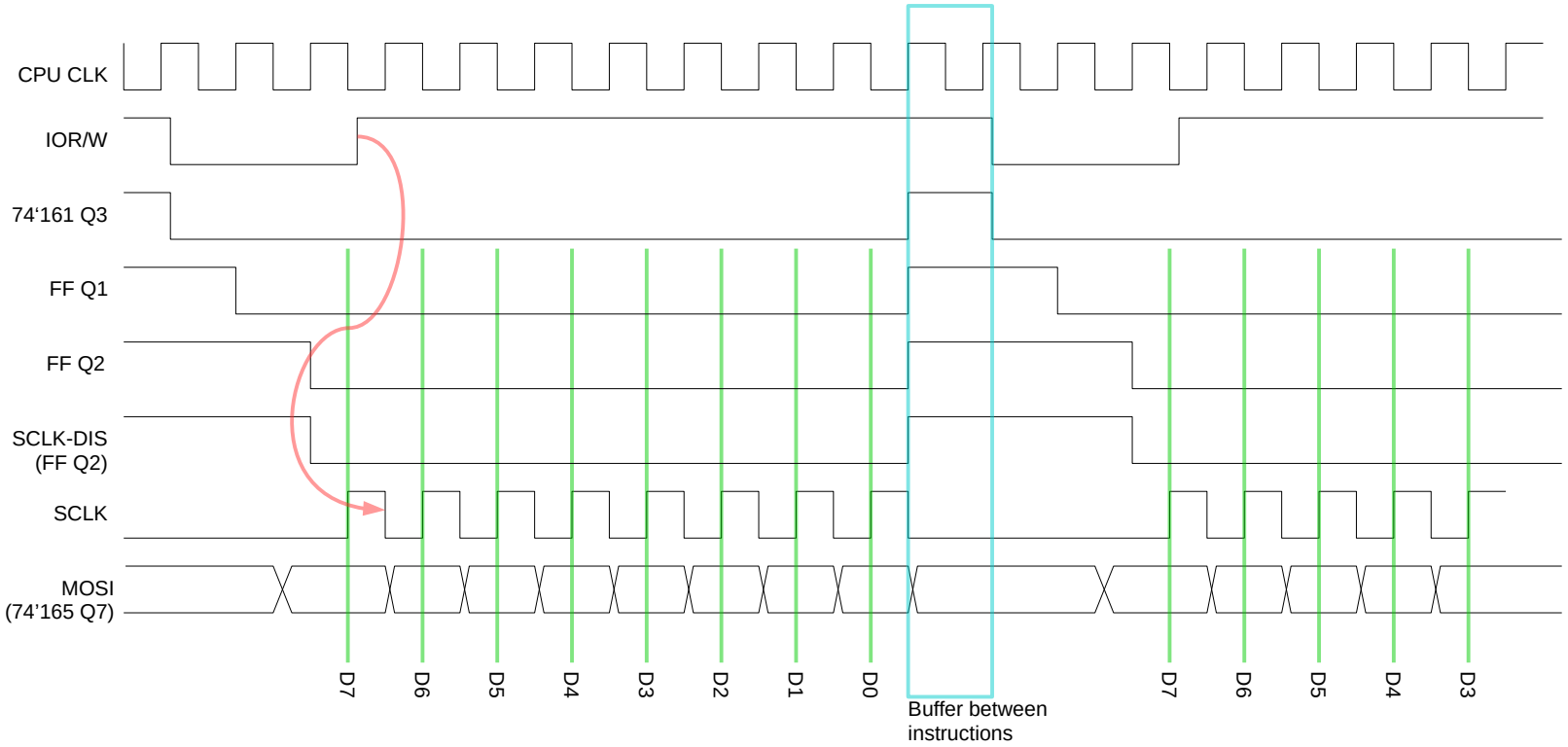
OUT instructions load the output data into the 74LS165 shift register. IN instructions read the data from the 74LS164 shift register. In both cases, the IO strobe will cause a /MR (reset the counter) which forces Q3 to "0" which is reflected by a "0" on the D input of the set of flipflops.

After two CPU clock pulses (rising edges) the "0" from Q3 should reach the Q output of the last flipflop, causing SCLK-DIS to be "0" and passing the CPU clock to the shift registers as well as the counter. Note that the exact timing of this depends on the Z80 CPU timing for I/O instructions, and is triggered by the leading edge of the IO strobe (IORD or IOWR). After 8 clock pulses, the counter will reach 1000b and Q3 will be "1" and this will force SCLK-DIS to a "1" again, stopping the shifting of data.

Note the critical timing for the trailing edge of /MR (IOR/W) and SCLK-DIS. The SCLK cycles actually begin while /MR is still active (74LS161 still held in reset), but this is acceptable because the trailing edge of /MR (counter reset released) occurs before the first counting edge (falling edge of SCLK) for the 74LS161. This overlap allows for a better buffer window between back-to-back I/O instructions.

Successive IN/OUT instructions cause the same 8-cycles of CPU clock to be passed through to the shift registers. Once the H8/H89 (software) has completed the command and data, it clears the control port - turning off any /SCS signal - which forces the preload (/PE) active again, preventing the counter from functioning.

H8/H89 SPI Timing (WIZ850io)



Example for back-to-back i8080 OUT/IN instructions.
Z80 I/O instructions are longer and provide more buffer time.
Red arrow indicates critical timing requirement.