**Diagnosing Kaypro Problems**
**using the**
**Kaypro Emergency Monitor ROM**
July 26, 2023

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## Introduction

Throughout this document, examples are shown using underlined text to indicate what the user types, and the token `(CR)` indicates pressing the RETURN or Enter key.

Diagnosing a broken Kaypro can be a complex and overwhelming task. This document attempts to break-down the task into steps, and gives examples of how to use the Emergency Monitor ROM to further diagnose problems.

This document picks up where the Emergency Monitor ROM documentation leaves off. That document should be read first.

The first step for a newly acquired Kaypro in unknown condition is to examine the electronics for signs of physical failure. A common failure is in electrolytic capacitors (as well as the RIFA capacitors). A thorough examination and testing of the power supplies and associated power components is beyond the scope of this document. This document begins once the power has been verified and the machine is safe to power-on and run.

In addition, a working CPU and main memory is required. One basic check for that is to run the Emergency Memory Test ROM. If the memory test is able to run but detects an error in RAM, then RAM should be replaced. If the memory test is unable to even run, that may indicate a bad CPU, which

must be replaced. However, this could also indicate a more-fundamental problem that requires diagnostics at an electronics level.

Be aware that earlier Kaypro models do not have sockets for all ICs. While the major ICs are socketed, many – include RAM – are not. This makes replacement much more difficult, at least the first time (until a socket is installed after desoldering the IC).

## Kaypro Model Identification

While there are ways to determine Kaypro features by using input/output commands on the monitor, the best way is to examine the mainboard, specifically noting the boot ROM part number and arrangement of ICs and rear-cabinet connectors. If a part number (81-XXX) can be located on the mainboard, that is the best way. Unfortunately, many boards have an assembly number visible, but not a part number. In addition, Kaypro has been known to re-spin the */84 mainboard with a different rear connector arrangement, also confusing identification. In some cases, the only difference between models is single vs. double sided drives, or whether the mainboard was fully-populated or not.

A valuable source for information on identifying Kaypro models is the Kaypro Technical Manual, available on bitsavers at http://www.bitsavers.org/pdf/kaypro/1484-F_Kaypro_Technical_Manual_Sep85.pdf But note that even this document does not enumerate all the variations actually produced by Kaypro, or that currently exist in the field. This document is also vital for performing in-depth diagnosis, as it contains schematics and other valuable materials.

The */83 models have only two rear connectors (parallel printer and serial data) with the keyboard jack between them. The */83 mainboards have only one Z80A-SIO/0 but two Z80A-PIOs and no 6545 CRT controller chip. The first-generation Kaypro II/83 models will only take a 2716 boot ROM, part number 81-149, while later */83 models can use a 2732 ROM with proper jumper placement and should have the 81-232 boot ROM. It is not known whether Kaypro ever built a */84 mainboard designed to (retro-)fit in a */83 case. If such a system exists, all procedures and software for the */84 models should be used in spite of outward appearances of being a */83. It should also be noted that the */83 video uses a 60Hz video sync, and is not compatible with the */84 and 10 model video boards (and vice versa).

The Kaypro 10, first generation, is an evolutionary step between */83 and */84. It contains most of the same hardware as */84, but does not provide for the modem or RTC circuits. It has two Z80A-SIO/0 and no Z80A-PIO chips, and has the 6545 (sometimes 6845E) CRT controller chip. It also does not have the custom gate arrays (81-189 and 81-194). This board has the 50-pin expansion (harddisk) connector near the middle of the board, and is missing locations for the telephonics (modem) transformer and RTC battery near the right edge. The boot ROM is 3732-only and uses 81-302. The rear connectors include parallel printer and two serial, with the light-pen and keyboard jacks on the far right. Later production Kaypro 10 models used the */84 mainboard, fabricated with the Kaypro 10 rear connector arrangement but replacing the light-pen jack with the modem. The Kaypro 10 (6545 CRTC) video uses 50Hz sync, and is not compatible with the */83 video boards (and vice versa).

The */84 models all have nearly-identical mainboards, with varying amounts populated. First generation 2/84 and 2X boards will have none of the modem, RTC, and harddisk populated (right region of the mainboard). Later production boards were fully populated. The rear connectors are similar to the Kaypro 10, except that the modem and keyboard jacks are on opposite ends of the serial and parallel connectors. These boards contain two Z80A-SIO/0, the 6545 (or 6845E) CRTC, and either space for or one actual Z80A-PIO – as well as circuitry for the modem and RTC. Floppy and harddisk connectors are arranged along the right edge. The original 2/84, 2X, and 4/84 boot ROM was 81-292. This was later changed to the "universal ROM" 81-478, which would automatically adapt to floppy-only, high-density floppy, and harddisk configurations and required CP/M 2.2u. The */84 (6545 CRTC) video uses 50Hz sync, and is not compatible with the */83 video boards (and vice versa).

## Memory/CPU Checks

One way to determine if basic CPU, ROM, and RAM are functional is to try the Emergency Memory Test ROM. This ROM will send output on the serial port as well as provide visual indicators that are visible from the front of the Kaypro. If neither the serial output nor the visual indicators are working, it may point to a CPU issue, or an issue addressing the ROM, or multiple failures of the serial port and the visual indicator for the Kaypro model being tested. These will require diagnostic methods not covered in this document.

## High-level Analysis

Determining "where to start looking" requires a basic understanding of the sequence of events performed by the boot ROM, combined with the symptoms presented by the machine. While different ROM versions perform steps differently, the basic sequence is:

1. Initialize SIO1 (keyboard and serial data)
2. Initialize/clear display
3. Setup common (BIOS) memory
4. Display signon message on screen
5. Initialize floppy, and boot if diskette present
6. [Kaypro 10] Initialize harddisk, and boot.
7. Fallback for failed boot (varies)

A general idea of how far the system gets can be guessed by checking for progress. For example, the video display RAM will power-on with garbage, so if the screen displays garbage characters then one can assume that the clear screen step was not completed. However, */83 machines have a video circuitry that requires no initialization and is always "on", in contrast to the */84 and 10 models that have a CRT controller chip which must be initialized before video will be enabled. If the CRTC has not been initialized and started, there will be no raster scan visible when the brightness is turned up.

Certainly, if the ROM signon message appears on the screen, the system has passed step 4 and it can be assumed that the CRTC and video is working.

Progress on booting from the floppy can be determined by observation. When attempting to boot, the ROM will select drive A and the drive motors will be spinning. Drives may or may not step to track 0, depending on the conditions when the system was last powered off. Some boot ROMs (at least 81-478) will show drive B selected for a moment, before switching to drive A and trying to boot (a side effect of testing to see if it is running on a Kaypro 10).

Also be aware that failure to boot could be caused by bad media or media that does not have the matching bootstrap code (or CP/M) for the ROM version.

## I/O Port Select Signals

One common question that arises when devices are not functioning is whether the chip-select signal is reaching the device. On the monitor, a simple program can be poked into memory and executed that will continuously pulse the desired chip-select, and then an oscilloscope can be used to confirm that the device is getting the select signal. The following example show the program, where the “XX” value should be replaced by the desire I/O port for the device to test.

```
: S 8000(CR)
8000 00 DB(CR)     (INPUT op-code)
8001 00 XX(CR)     (replace XX with desired port)
8002 00 C3(CR)     (JUMP op-code)
8003 00 00(CR)     (low byte of 8000H)
8004 00 80(CR)     (high byte of 8000H)
8005 00 .
: G 8000(CR)
GO 8000 ?Y
```

It will be necessary to RESET the Kaypro in order to get back to the monitor prompt.

Following are the I/O ports for the various Kaypro models. Note that some Kaypro 10s are fitted with the */84 mainboard. Also note that some */84 models do not have the PIO, RTC, and Modem electronics.

| Port Adr | */83 | | 10 | | */84 | |
|---|---|---|---|---|---|---|
| | **Device** | **Function** | **Device** | **Function** | **Device** | **Function** |
| 00 | WD1943 Baud Gen. Serial I/O | baud | WD1943 Baud Gen. Serial Data | baud | WD1943 Baud Gen. Serial Data | baud |
| 01 | | | | | | |
| 02 | | | | | | |
| 03 | | | | | | |
| 04 | Z80-SIO Serial I/O Keyboard | ch A data | Z80-SIO #1 Serial Data Keyboard | ch A data | Z80-SIO #1 Serial Data Keyboard | ch A data |
| 05 | | ch B data | | ch B data | | ch B data |
| 06 | | ch A ctl | | ch A ctl | | ch A ctl |
| 07 | | ch B ctl | | ch B ctl | | ch B ctl |
| 08 | Z80-PIO #1 Printer | ch A data | WD1943 Baud Gen. Serial Printer | baud | WD1943 Baud Gen. Serial Printer | baud |
| 09 | | ch B data | | | | |
| 0A | | ch A ctl | | | | |
| 0B | | ch B ctl | | | | |
| 0C | WD1943 Baud Gen. Keyboard | baud | Z80-SIO #2 Serial Printer | ch A data | Z80-SIO #2 Serial Printer Modem | ch A data |
| 0D | | | | ch B data | | ch B data |
| 0E | | | | ch A ctl | | ch A ctl |
| 0F | | | | ch B ctl | | ch B ctl |
| 10 | WD1793 Floppy Controller | cmd/sts | WD1793 Floppy Controller | cmd/sts | WD1793 Floppy Controller | cmd/sts |
| 11 | | track | | track | | track |
| 12 | | sector | | sector | | sector |
| 13 | | data | | data | | data |
| 14 | N/C | | SysPort | sysprt | SysPort | sysprt |
| 15 | | | | | | |
| 16 | | | | | | |
| 17 | | | | | | |
| 18 | N/C | | Parallel Printer | data out | Parallel Printer | data out |
| 19 | | | | | | |
| 1A | | | | | | |
| 1B | | | | | | |
| 1C | Z80-PIO #2 SysPort | ch A data | 6545A-1 CRT Controller | ctl/sts | 6545A-1 CRT Controller | ctl/sts |
| 1D | | ch B data | | data | | data |
| 1E | | ch A ctl | | | | |
| 1F | | ch B ctl | | vid RAM | | vid RAM |

| Port Adr | */83 | | 10 | | */84 | |
|---|---|---|---|---|---|---|
| | Device | Function | Device | Function | Device | Function |
| 20 | N/C | | N/C | | Z80-PIO RTC Modem | ch A data |
| 21 | | | | | | ch B data |
| 22 | | | | | | ch A ctl |
| 23 | | | | | | ch B ctl |
| 24 | N/C | | N/C | | RTC | data |
| 25 | | | | | | |
| 26 | | | | | | |
| 27 | | | | | | |
| 80 | N/C | | WD1002-HDO Controller | data | N/C | |
| 81 | | | | error | | |
| 82 | | | | sec count | | |
| 83 | | | | sector | | |
| 84 | | | | cyl low | | |
| 85 | | | | cyl high | | |
| 86 | | | | SDH | | |
| 87 | | | | cmd/sts | | |

When doing chip-select testing, a specific port should be chosen for the least side-effects. For example, reading from most ports has no serious side-effect, but writing to a port could significantly alter the system behavior.

## SysPort Usage

Note that the sysport contains the “bank” control on bit 7. It is imperative that this bit never be set to “0” (unless by a special program running in high memory), as that would make the ROM code disappear and the system would crash.

The general practice with SysPort is to read the current value, modify it, then write the new value. In this environment, there should be no hidden changes to the port and so it is reasonable to just know what the right value is without reading the port.

The main operations needed on the sysport are to turn on/off the motors and select a drive (or deselect all). While the sysport bit numbers involved with these actions are same for all models, the actual values used are not.

### *Model */83 SysPort*

The */83 models use a different system port (Z80-PIO) than the others, and this port must be initialized before it can be used. Do not perform this initialization on a */84 or 10 model, as it will corrupt the

CRTC registers. The Z80-PIO resets to a state where all data lines are inputs, effectively causing them to float “1”. This places the lines, especially BANK, in the correct state for the system to run until the sysport is configured and enabled. The safe way to enable the */83 sysport is:

```
: O 1C C0(CR)       (make certain BANK stays on)
: O 1D CF 08(CR)    (init and activate PIO ch A)
:
```

This sequence leaves motor off and no drive selected. The floppy-related sysport bits (expressed as hexadecimal mask) are:

| | | | |
|---|---|---|---|
| */83 (PIO 1CH) | Drive A select | 01 | 1=select |
| | Drive B select | 02 | 1=select |
| | Side select | 04 | 1=side-1 |
| | DD enable | 20 | 0=DD |
| | Motor control | 40 | 0=ON |

As an example, outputting the value 81 to port 1C (after initializing the PIO) would select drive A, side 0, motor ON, and enable double-density.

### *Models */84 and 10 SysPort*

On */84 and 10 models, the sysport RESETs (and powers on) to a special state where all outputs are tri-state and float high (“1”). The first write to sysport will also turn off this state and enable the sysport outputs. So, the first read of sysport (before any write) will return the tri-state values – not the actual state of the bits in the latch. Also note that the parallel printer “ready” bit will never read as the state of the “A12 CH” output. This bit may initially read “0” or “1” depending on whether there is a printer connected, and powered on, at the parallel printer port. The “A12 CH” output is generally not functional (“don’t care”), unless a special character generator ROM has been installed for the CRTC.

Here are the disk-related sysport bits (expressed as hexadecimal mask) for the two families:

| | | | |
|---|---|---|---|
| Kaypro 10 (port 14H) | Drive A select | 01 | 0=select |
| | WD1002 reset | 02 | 1=reset |
| | Side select | 04 | 0=side-1 |
| | Motor control | 10 | 1=ON |
| | DD enable | 20 | 0=DD |
| */84 (port 14H) | Drive A select | 01 | 0=select |
| | Drive B select | 02 | 0=select |
| | Side select | 04 | 0=side-1 |

| | | | |
|---|---|---|---|
| | Motor control | 10 | 1=ON |
| | DD enable | 20 | 0=DD |

Note that the main difference between models 10 and */84 is the re-assignment of Drive B select to WD1002 RESET.

As an example, outputting the value DE to port 14 would select drive A, side 0, motor ON, and enable double-density.

## Display Diagnosis

### *Model */83 Display*

The model */83 video display is made using discrete logic (there is no controller chip). The system powers on with video enabled, and should be producing a raster on the CRT immediately. Diagnosing the video circuitry (no raster, or malformed raster) is beyond the scope of this document. If the display does start up correctly, probably the most likely issue would be video RAM and should be noticeable by incorrect characters on the screen. With the monitor ROM installed, the video RAM is not cleared on power-up or RESET and so will contain garbage (or the previous contents after RESET). The video RAM may be accessed directly from the monitor at addresses 3000H-3BFFH, and so various patterns can be written to video RAM and the effects can be viewed on the display. Each display line begins on a 128B boundary, but only 80 characters of RAM are used. Addresses in the latter part of the 128B region are mapped over the 80 character display line, but otherwise cause no problem. Typically, the F(ill), S(ubstitute), and M(ove) commands are useful for exploring video RAM, in addition to D(ump) for verifying contents. For example, the command “F 3000 3BFF 20” will clear the display. By analyzing the resulting display after filling video RAM with a given value, errors can be seen. Note that bit 7 controls blink, while bits 6-0 select which character to display. The top half of the display is controlled by U29 (bits 7-4) and U30 (bits 3-0), while the bottom half is controlled by U28 (bits 7-4) and U31 (bits 3-0).

### *Model */84 and 10 Display*

The model */84 and 10 systems use a 6545A-1 CRT Controller chip. This chip powers-up with video disabled, and no raster will be present on the screen until the CRTC is programmed. The video RAM is not directly accessible from the monitor, but will be filled with garbage after power-on. Note that the 6845E is sometimes used as a replacement for the 6545, but beware that without the “E” suffix the part is not compatible and won’t work.

The first test is to program the CRTC and see whether the screen lights up with garbage characters.

```
: N CRTC(CR)        (display should light up)
```

If the display does not light up after this command, then the CRTC will need to be further tested to determine where the problem might be. The first test is to check if the CRTC “Update” status working correctly. This is used by the Kaypro ROMs to read or write video RAM without disrupting the display refresh. This command checks whether the Update status is seen to toggle through three update cycles:

```
: T CRTC(CR)
Wait... Update Update Update
```

This command will “hang” if an update does not occur, but may be interrupted by pressing any key.

The next step would be to check that the vertical retrace is occurring, and at the correct rate. This generally confirms that all other timing is correct.

```
: T VRT(CR)
80 001C
A0 064B
80 06AF
A0 0CDE
80 0D42
A0 1371
80 13D5
A0 1A03
80 1A68
A0 2096
```

This command does not normally run the full cycle (iteration count FFFF), instead stopping after 10 status register changes. If it does reach the FFFF count, it probably indicates a problem in the CRTC. Vertical retrace is in bit 5 (20 hex) of the status register. The above data shows that we see retrace at 064B and 0CDE (among other times). Subtracting those gives 0693 hex or 1683 decimal. That computes to approximately 20 mS which matches the desired 50Hz vertical retrace rate.

If all these tests pass and the display is still not working, there may be problems outboard of the CRTC, possibly on the video board. Beware of high voltage.

There is a command that will fill video RAM with a character, and also set the attributes. This can be used to do some testing of the video RAM, by setting certain values and observing whether the display looks correct. The general command syntax is:

**T CRTF** [*char* [*attr*]]

Where char is the hexadecimal value to put in all character locations and attr is the hexadecimal attributes value to apply to all locations. Attribute bits are: 01=reverse, 02=dim, 04=blink, 08=underline. The defaults are the blank space character and 00 attributes, effectively a clear screen.

There are only two video RAM chips on these models:

**10/83:** U35 controls the characters and U44 controls the attributes.

***/84:** U23 controls the characters and U15 controls the attributes.

If wrong characters are being displayed, that suggests that the character RAM needs to be replaced. If wrong attributes are shown, that suggests attribute RAM. There could be other causes for a wrong display, though. Also, bad RAM could be intermittent or possibly sensitive to patterns in adjacent locations.

## Floppy Diagnosis

NOTE: Most of the following commands require that a floppy drive be selected. Refer to section “SysPort Usage” for information about floppy drive select and control signals. The exact procedure, and value, is different depending on the Kaypro model.

If floppy drive select and motor control seem to be working, the next step would be to confirm that the controller chip is functioning at a basic level. This can be done by performing the FLPY test command, which will issue a FORCE INTERRUPT command to the controller and watch for the expected results.

At this point, an overview of the WD1793 status register bits is in order. The status registers bits may have one of two possible meanings depending on the command that was last run. After head-movement commands, and force-interrupt, the status register bits are:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NRDY | WP | HLD | SEEK ERR | CRC ERR | TRK00 | INDEX | BUSY |

For read/write commands, the status register bits are:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NRDY | WP | FAULT* | RNF | CRC ERR | LOST DAT | DRQ | BUSY |

Note that the Kaypro hard-wires the READY and HLD signals, so NRDY should always be “0”.

Here are the expected results of running the FLPY command when no drive is selected:

```
: T FLPY(CR)
01 0002
00 0003
00 FFFF
```

The expected results, above, show that the BUSY bit went on briefly in response to the command, and then stayed off. The key result is that the BUSY bit is still off when the iteration count FFFF is reached.

If this controller is handling the FORCE INTERRUPT command correctly, there may some issue with signals from the drives reaching, and passing through, the controller. The first of these is the TRK00

signal, which indicates that the selected drive's heads are on track 0. This will require that a drive be selected, but no diskette need be in the drive (the head protectors should be removed, though). Selecting a floppy driveThe test involves performing a RESTORE command and confirming that the TRK00 signal shows up in the status register, then stepping in and confirming that TRK00 goes off, then RESTORE again and confirming TRK00 is back on:

```
: O 10 03(CR)       (RESTORE - make sure drive is at track 0)

: I 10(CR)
Input 10 = 46       (confirm TRK00 bit (04) is on)

: T FLPY 53(CR)     (send STEP IN command)
47 0002             (BUSY on, TRK00 on)
43 00A4             (TRK00 goes off as head steps away)
42 09A8             (command done)
42 FFFF

: T FLPY 03(CR)     (send RESTORE command)
43 0002             (BUSY on)
47 28C4             (TRK00 on)
46 30FD             (command done)
46 FFFF
```

Note that the INDEX signal (02) and WP (40) are always on in this case, because there is no diskette in the drive and the sensors are not obstructed.

If the TRK00 signal is not working correctly, it will be necessary to trace that signal to the WD1793 pin 34 from the drive (pin 26 on the drive connector)

The next check is for the INDEX signal from a spinning diskette. The Kaypro boot ROMs check this signal before deciding to boot. Insert a diskette into the drive and close the door. The diskette need not be formatted.

The following command watches the status register and records any changes, which should only involve the INDEX signal.

```
: T FLPY(CR)        (issue default command, FORCE INTR)
05 0002             (BUSY on for command)
04 0003             (BUSY off)
06 1441             (INDEX (02) on)
04 159D             (INDEX off)
06 5572             (INDEX on)
04 56CE
06 96A3
04 97FF
06 D7D4
04 D930
04 FFFF
```

If the output shows the INDEX signal working, a further test is to measure the time between INDEX pulses. In this case, we see INDEX start at 1441 and 5572. We subtract those to get 4131 hex, or 16689 decimal. This computes out to 200.268 mS (4MHz Z80), which is plenty close enough to 300 RPM.

The next step is to try and read the boot sector off the diskette. With the heads at track 0, set the side and double-density bits correctly (typically double-density, always side 0). This diskette must be bootable in order to see a valid boot sector, and (of course) must be formatted at the very least.

For drive A on a model */84 or 10, the sysport value would be DE. For drive A on model */83, the sysport value would be 81.

The following commands read and dump the boot sector. The exact contents of this sector will vary between CP/M versions, but should look similar.

```
: T FDRD 00(CR)    (perform READ of sector 0)
00                 (no error detected)
: D8000 81FF(CR)   (dump sector buffer)
8000 18 FE 00 E4 00 FA 30 00 00 00 00 00 00 00 00 00   ......0.........
8010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8050 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8080 C3 5C E7 C3 58 E7 7F 01 44 00 20 20 20 20 20 20   .\..X...D.
8090 20 20 20 20 20 20 20 20 43 4F 50 59 52 49 47 48           COPYRIGH
80A0 54 20 28 43 29 20 31 39 37 39 2C 20 44 49 47 49   T (C) 1979, DIGI
80B0 54 41 4C 20 52 45 53 45 41 52 43 48 20 20 00 00   TAL RESEARCH  ..
80C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8100 00 00 00 00 00 00 00 00 08 E4 00 00 5F 0E 02 C3   ............_...
8110 05 00 C5 CD 8C E4 C1 C9 3E 0D CD 92 E4 3E 0A C3   ........>....>..
8120 92 E4 3E 20 C3 92 E4 C5 CD 98 E4 E1 7E B7 C8 23   ..> ........~..#
8130 E5 CD 8C E4 E1 C3 AC E4 0E 0D C3 05 00 5F 0E 0E   ............_...
8140 C3 05 00 CD 05 00 32 EE EB 3C C9 0E 0F C3 C3 E4   ......2..<......
8150 AF 32 ED EB 11 CD EB C3 CB E4 0E 10 C3 C3 E4 0E   .2..............
8160 11 C3 C3 E4 0E 12 C3 C3 E4 11 CD EB C3 DF E4 0E   ................
8170 13 C3 05 00 CD 05 00 B7 C9 0E 14 C3 F4 E4 11 CD   ................
8180 EB C3 F9 E4 0E 15 C3 F4 E4 0E 16 C3 C3 E4 0E 17   ................
8190 C3 05 00 1E FF 0E 20 C3 05 00 CD 13 E5 87 87 87   ......  ........
81A0 87 21 EF EB B6 32 04 00 C9 3A EF EB 32 04 00 C9   .!...2...:..2...
81B0 FE 61 D8 FE 7B D0 E6 5F C9 3A AB EB B7 CA 96 E5   .a..{.._.:......
81C0 3A EF EB B7 3E 00 C4 BD E4 11 AC EB CD CB E4 CA   :...>...........
81D0 96 E5 3A BB EB 3D 32 CC EB 11 AC EB CD F9 E4 C2   ..:..=2.........
81E0 96 E5 11 07 E4 21 80 00 06 80 CD 42 E8 21 BA EB   .....!.....B.!..
81F0 36 00 23 35 11 AC EB CD DA E4 CA 96 E5 3A EF EB   6.#5.........:..
```

If no problem has been found, one last thing to check here is that side 1 is also readable (and returns different data). Here we will read the first directory sector of the drive. This requires changing the sysport value to select side 1. For model */84 and 10, the value should be DA. For */83, it should be 85. The sector number also changes to 0A.

```
: T FDRD 0A(CR)
00
: D8000 81FF(CR)
8000 00 4D 4F 56 43 50 4D 20 20 43 4F 4D 00 00 00 4C   .MOVCPM  COM...L
8010 02 03 04 05 06 00 00 00 00 00 00 00 00 00 00 00   ................
8020 00 50 49 50 20 20 20 20 20 43 4F 4D 00 00 00 3A   .PIP     COM...:
8030 07 08 09 0A 00 00 00 00 00 00 00 00 00 00 00 00   ................
8040 00 53 55 42 4D 49 54 20 20 43 4F 4D 00 00 00 0A   .SUBMIT  COM....
8050 0B 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8060 00 58 53 55 42 20 20 20 20 43 4F 4D 00 00 00 06   .XSUB    COM....
8070 0C 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8080 00 45 44 20 20 20 20 20 20 43 4F 4D 00 00 00 34   .ED      COM...4
8090 0D 0E 0F 10 00 00 00 00 00 00 00 00 00 00 00 00   ................
80A0 00 41 53 4D 20 20 20 20 20 43 4F 4D 00 00 00 40   .ASM     COM...@
80B0 11 12 13 14 00 00 00 00 00 00 00 00 00 00 00 00   ................
80C0 00 44 44 54 20 20 20 20 20 43 4F 4D 00 00 00 26   .DDT     COM...&
80D0 15 16 17 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80E0 00 53 54 41 54 20 20 20 20 43 4F 4D 00 00 00 29   .STAT    COM...)
80F0 18 19 1A 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8100 00 53 59 53 47 45 4E 20 20 43 4F 4D 00 00 00 08   .SYSGEN  COM....
8110 1B 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8120 00 44 55 4D 50 20 20 20 20 41 53 4D 00 00 00 21   .DUMP    ASM...!
8130 1C 1D 1E 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8140 00 43 4F 50 59 20 20 20 20 43 4F 4D 00 00 00 3C   .COPY    COM...<
8150 1F 20 21 22 00 00 00 00 00 00 00 00 00 00 00 00   . !"............
8160 00 53 53 43 4F 50 59 20 20 43 4F 4D 00 00 00 3C   .SSCOPY  COM...<
8170 23 24 25 26 00 00 00 00 00 00 00 00 00 00 00 00   #$%&............
8180 00 54 45 52 4D 20 20 20 20 43 4F 4D 00 00 00 06   .TERM    COM....
8190 27 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   '...............
81A0 00 53 42 41 53 49 43 20 20 43 4F 4D 01 00 00 4C   .SBASIC  COM...L
81B0 28 29 2A 2B 2C 2D 2E 2F 30 31 32 33 34 00 00 00   ()*+,-./01234...
81C0 00 4F 56 45 52 4C 41 59 42 43 4F 4D 00 00 00 36   .OVERLAYBCOM...6
81D0 35 36 37 38 00 00 00 00 00 00 00 00 00 00 00 00   5678............
81E0 00 42 41 53 49 43 4C 49 42 52 45 4C 01 00 00 80   .BASICLIBREL....
81F0 39 3A 3B 3C 3D 3E 3F 40 41 42 43 44 45 46 47 48   9:;<=>?@ABCDEFGH
```

The exact data returned will depend on the contents of the directory, and may not contain any file names at all if the diskette is empty. But, the data should be different than the boot sector. Since sectors are numbered differently between side 0 and side 1, it should not be possible to read the wrong side (e.g. if the side-select signal were broken or shorted). The error from the FDRD command in that case would normally be 10 (record not found).

Failure to read media could be caused by many things, but perhaps the most common is a failure of the WD9216 data separator. If a drive is selected, motor on, and diskette inserted there should be a continuous stream of read data transmitted. It should be possible to probe along the read data path with

an oscilloscope and perhaps determine where things are going wrong. A signal integrity problem may be more difficult to track down.

## Harddisk Diagnosis

The first test is to see if the Kaypro can communicate with the WD1002 controller, and whether the controller can pass it's self test. The controller is reset, which causes it to run the self test. The result will tell whether the reset was affective and whether the self test passed.

```
: N HDD(CR)  (reset WD1002, starts self test)
85 0000
80 C737
00 C73C
01           (expected error code)
```

Because the WD1002 in the Kaypro 10 has no floppy support, the self test will always end with code 01. This code means that the WD2797 failed to pass the tests, which is expected since it is not installed.

According to the WD1002-05/HDO documentation, these are the possible error codes from the self test:

| | |
|---|---|
| 05 | WD1015 Error |
| 04 | WD1014 or Bus Error |
| 03 | Sector Buffer Error |
| 02 | WD1010 Error |
| 01 | WD2797 Error |
| 00 | Pass – WD1002 is functional |

If the self test passes, then a test of reading the media is in order. To read the boot sector (cylinder 0, head 0, sector 0), perform the following

```
: O 86 A8(CR)      (SDH: CRC, 512B, drv 2, head 0)

: O 82 01(CR)      (sector count 1)

: O 83 00(CR)      (sector 0)

: O 84 00(CR)      (cylinder XX00)

: O 85 00(CR)      (cylinder 00XX)

: T HDD 20(CR)     (issue READ command)
D0 0000
58 02B8            (DRQ, waiting for xfer)
00                 (no errors yet)
: T HDRD(CR)       (perform xfer)
```

```
8200
: D 8000 81FF(CR) (dump the data)
8000 18 FE 00 D8 00 EE 37 00 00 00 00 00 00 00 00   ......7.........
8010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8050 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8070 00 00 00 00 00 00 00 00 00 00 00 00 00 13 03   ................
8080 C3 5C DB C3 58 DB 7F 00 20 20 20 20 20 20 20   .\..X...        .
8090 20 4D 41 53 4D 45 4E 55 00 43 4F 50 59 52 49 47    MASMENU.COPYRIG
80A0 48 54 20 28 43 29 20 31 39 37 39 2C 20 44 49 47   HT (C) 1979, DIG
80B0 49 54 41 4C 20 52 45 53 45 41 52 43 48 20 00 00   ITAL RESEARCH ..
80C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8100 00 00 00 00 00 00 00 00 08 D8 00 00 5F 0E 02 C3   ............_...
8110 05 00 C5 CD 8C D8 C1 C9 3E 0D CD 92 D8 3E 0A C3   ........>....>..
8120 92 D8 3E 20 C3 92 D8 C5 CD 98 D8 E1 7E B7 C8 23   ..> ........~..#
8130 E5 CD 8C D8 E1 C3 AC D8 0E 0D C3 05 00 5F 0E 0E   ............_..
8140 C3 05 00 CD 05 00 32 EE DF 3C C9 0E 0F C3 C3 D8   ......2..<......
8150 AF 32 ED DF 11 CD DF C3 3F EE 0E 10 C3 C3 D8 0E   .2......?.......
8160 11 C3 C3 D8 0E 12 C3 C3 D8 11 CD DF C3 DF D8 0E   ................
8170 13 C3 05 00 CD 05 00 B7 C9 0E 14 C3 F4 D8 11 CD   ................
8180 DF C3 F9 D8 0E 15 C3 F4 D8 0E 16 C3 C3 D8 0E 17   ................
8190 C3 05 00 1E FF 0E 20 C3 05 00 CD 13 D9 87 87 87   ...... .........
81A0 87 21 EF DF B6 32 04 00 C9 3A EF DF 32 04 00 C9   .!...2...:..2...
81B0 FE 61 D8 FE 7B D0 E6 5F C9 3A AB DF B7 CA 96 D9   .a..{.._.:......
81C0 3A EF DF B7 3E 00 C4 BD D8 11 AC DF CD CB D8 CA   :...>...........
81D0 96 D9 3A BB DF 3D 32 CC DF 11 AC DF CD F9 D8 C2   ..:..=2.........
81E0 96 D9 11 07 D8 21 80 00 06 80 CD 42 DC 21 BA DF   .....!.....B.!..
81F0 36 00 23 35 11 AC DF CD DA D8 CA 96 D9 3A EF DF   6.#5.........:..
```

The exact data will depend on the version of CP/M, and whether the drive was even SYSGEN'ed. If the drive is not even formatted, the read will not succeed. Of course, the media could be bad (or heads crashed) such that nothing can be read.

WARNING: This is a destructive test, but one can issue the WD1002 format command for a track, and then see if the new sector(s) can be read.

Data layout differs depending on the ROM version that created it. Data stored on an HDD using ROM 81-302 cannot be accessed from ROM 81-478. This monitor does not care about the layout, but one must know which sectors to access when looking for specific data.

The harddisk geometry on original Kaypro drives is 306 cylinders, 4 heads, 17 sectors per track, 512 byte sectors.

### *ROM 81-302 HDD Layout*

Here are the logical tracks (for a drive) and their use. '*' indicates a mirrored track.

| **Cylinder** | **Heads** | | | | **Notes** |
|---|---|---|---|---|---|
| | **Drive A** | | **Drive B** | | |
| | **0** | **1** | **2** | **3** | |
| **0** | 0 | 1 | 0 | 1 | Boot tracks and ??? |
| **1** | 2 | 3 | 2 | 3 | |
| **2** | 4 | 4* | 4 | 4* | CP/M Directory area |
| **3** | 5* | 5 | 5* | 5 | |
| **4** | 6 | 6* | 6 | 6* | |
| **5** | 7* | 7 | 7* | 7 | |
| **6** | 8 | 9 | 8 | 9 | CP/M File Data blocks |
| **7** | 10 | 11 | 10 | 11 | |
| **8** | 12 | 13 | 12 | 13 | |
| **...** | ... | ... | ... | ... | |
| **303** | 602 | 603 | 602 | 603 | |
| **304** | 604 | 605 | 604 | 605 | |
| **305** | - | - | - | - | Parking |

The CP/M DPB used for both A and B is:

68 sectors per track
4K block size
2 extents per directory entry
1126 blocks total space
1024 directory entries
8 reserved directory blocks
4 reserved (boot) tracks

### *ROM 81-478 HDD Layout*

Here are the logical tracks (for a drive) and their use. The spare track table is maintained on cylinder 0 head 0 sector 16.

| Cylinder | Heads | | | | Notes |
|---|---|---|---|---|---|
| | Drive A | | Drive B | | |
| | 0 | 1 | 2 | 3 | |
| **0** | 0 | 1 | spare | spare | Boot track and spares table |
| **1** | spare | spare | spare | spare | |
| **2** | spare | spare | spare | spare | |
| **3** | spare | spare | spare | spare | |
| **4** | spare | spare | spare | spare | |
| **5** | spare | spare | spare | spare | |
| **6** | spare | spare | 0 | 1 | |
| **7** | 2 | 3 | 2 | 3 | CP/M Directory and File Data blocks area |
| **8** | 4 | 5 | 4 | 5 | |
| **9** | 6 | 7 | 6 | 7 | |
| **...** | ... | ... | | | |
| **303** | 594 | 595 | 594 | 595 | |
| **304** | 596 | 597 | 596 | 597 | |
| **305** | - | - | - | - | Parking |

The CP/M DPB used for both A and B is:

68 sectors per track
4K block size
2 extents per directory entry
1126 blocks total space
1024 directory entries
8 reserved directory blocks
2 reserved (boot) tracks

## Keyboard Diagnosis

The keyboard is attached by a serial port, using 300 baud. This port must be initialized before the keyboard can be tested. Initialization is slightly different for */83 models compared to later models, so there are two different commands. Choose the command for the model being tested. In this example, the system under test is a */84 or 10.

```
: N KB84(CR)          (initialize keyboard port on */84 and 10 models)
```

or for */83 models:

```
: N KB83(CR)          (initialize keyboard port on */83 models)
```

The communication path from Kaypro to the keyboard (only used to sound the “beep”) can be tested by send a Ctrl-D character out the serial port. This should cause the keyboard to “beep”.

```
: O 05 04(CR)
                      (keyboard beeps)
:
```

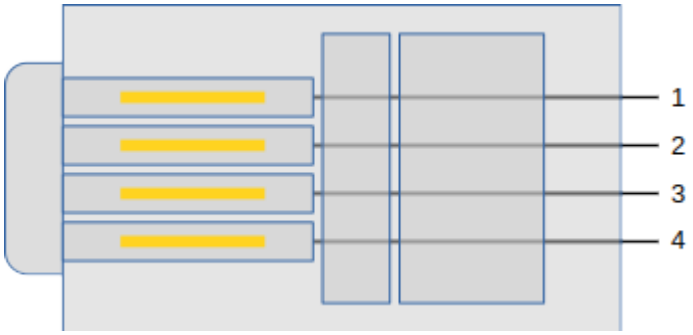
The following test will receive keycodes from the keyboard as you type them (press the keys). The keycodes are printed in hexadecimal. You may end the test by pressing any key on the monitor console.

```
: T KBD(CR)           (start keyboard test, press keys on keyboard)
Wait... 61 73 64 66 77 65 65 72 F3 F4 (CR)Abort
:
```

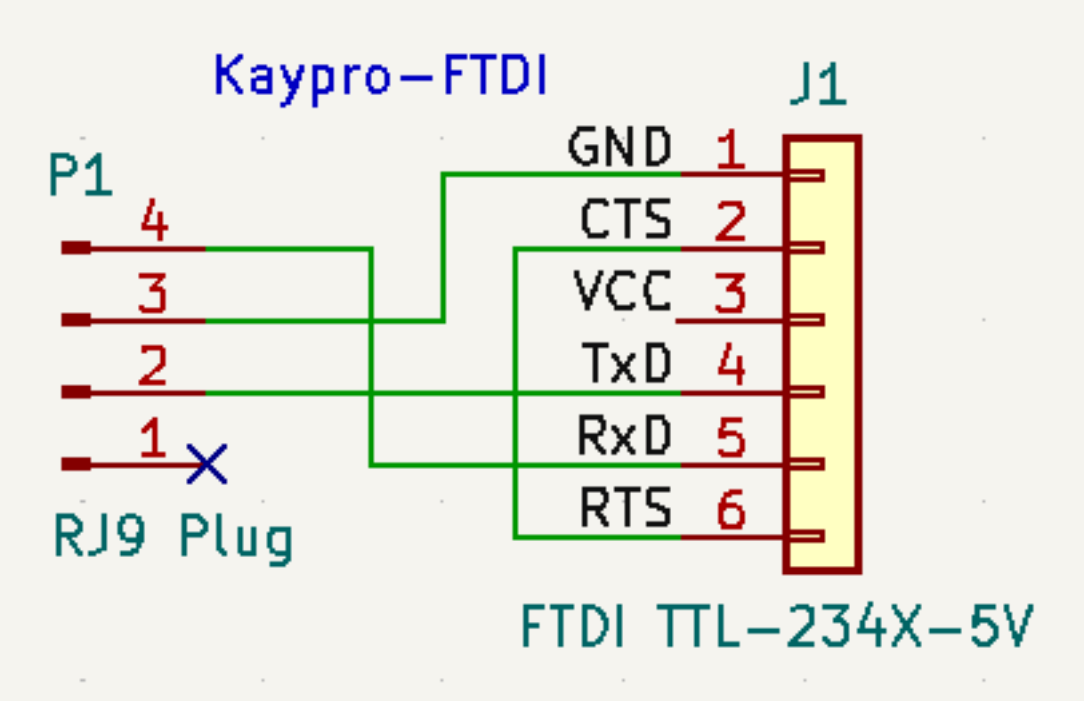
Since the monitor console runs on channel A of the same SIO, it may be less likely that channel B would be bad independent of channel A. One check to be done is to confirm that the baud clock is working. The signal on the SIO pin 27 should be 4800Hz (16x300 baud). On */83 models, this signal comes from the WD1943 “transmit” channel. On */84 models, it is hardwired to a 4800Hz source coming from the memory controller chip, the 81-194. On Kaypro 10 models, it is generated by counters from the CPU clock. Note that replacing the SIO requires that the correct variation be used. The Kaypro uses only the Z80A-SIO/0 variation.

The keyboard and Kaypro “keyboard port” can be tested separately, using a USB-Serial dongle such as the FTDI TTL-234X-5V. Be careful to only use the TTL and 5V variety. Plugging true RS-232 +/-12V signals into the keyboard ports can damage them.

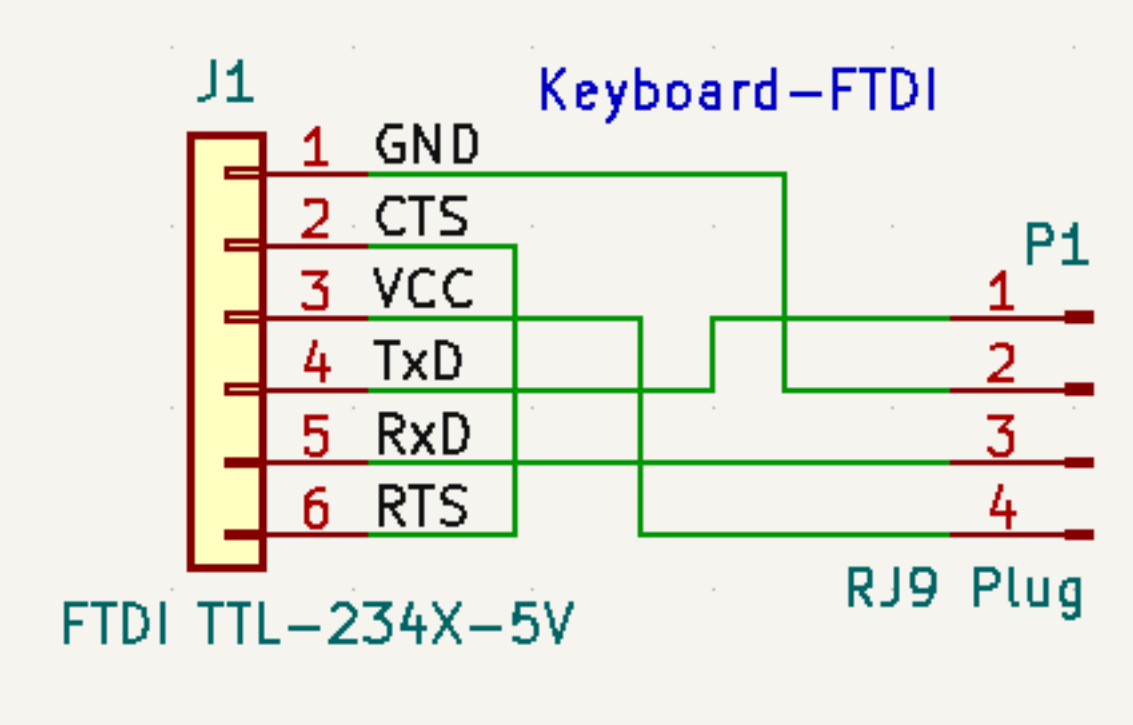
The RJ9 connectors have pin 1 on the right side, when viewing the contact side of the plug:



Here is the connection used for testing the Kaypro “keyboard port”:




Here is the connection used for testing the keyboard:




Note that the Kaypro uses a reversing cable with RJ9 connectors (equivalent to a telephone handset cable). This means that pin 1 of the Kaypro RJ9 jack connects to pin 4 of the keyboard RJ9 jack. This is

the reason that the FDTI connections are different depending on whether connecting to the Kaypro or the keyboard.

Also note that the Kaypro supplies +5V to the keyboard, and the FTDI cable is also supplying +5V. This is why +5V is left unconnected to the Kaypro. However, the keyboard requires external +5V to operate, and so the FTDI cable must connect the +5V. This also requires that a powered USB jack on the computer (or hub) be used, in order to supply the power needed by the keyboard.

With connections made, start up a terminal program on the USB serial device. Remember to set the port to 300 baud.

When connected to the Kaypro, you can run the “T KBD” command and type characters on the terminal program and see them received. You can also use “O 05 XX”, where “XX” is the desired ASCII code in hexadecimal, to send characters to the terminal program.

When connected to the keyboard, typing characters on the keyboard should be received by the terminal program. You can also press Ctrl-D on the terminal program to make the keyboard “beep”.

Testing the Kaypro keyboard serial port (Z80-SIO) separately from the keyboard itself would allow isolation of a problem to either the keyboard unit or the Kaypro (Z80-SIO and drivers/receivers).